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Clean Version of Pending Claims

STRUCTURE AND METHOD FOR DUAL GATE OXIDE THICKNESSES
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Claims 33-40 and 55-86, as of February 12, 2002 (date response to Final Office Action filed w/ RCE).

1 ~~33~~. (Amended) A logic device and a memory device structure on a single substrate, comprising:

a first transistor having a source and a drain region in the substrate separated by a channel region in the substrate, wherein the first transistor includes a dielectric layer of a first thickness, including a top layer which exhibits a high resistance to oxidation at high temperatures, separating a gate from the channel region; and

a second transistor having a source and a drain region in the substrate separated by a channel region in the substrate, wherein the second transistor includes a dielectric layer of second thickness different from the first thickness, separating a gate from the channel region.

2 1 ~~34~~. The structure of claim ~~33~~, wherein the first transistor is a transistor for the logic device and the second transistor is a transistor for the memory device.

3 1 ~~35~~. The structure of claim ~~33~~, wherein the first transistor having a dielectric layer of a first thickness includes a dielectric layer having a thickness of less than 7 nanometers.

4 1 ~~36~~. The structure of claim ~~33~~, wherein the first transistor having a dielectric layer of a first thickness includes a bottom layer of silicon dioxide (SiO_2) and a top layer of silicon nitride (Si_3N_4).

5 1 ~~37~~. The structure of claim ~~35~~, wherein the second transistor having a dielectric layer of second thickness includes a dielectric layer formed entirely of silicon dioxide (SiO_2).

~~38~~ 6. The structure of claim ~~33~~ 1, wherein the second transistor having a dielectric layer of second thickness includes a dielectric layer having a thickness of less than 12 nanometers.

~~39~~ 7. The structure of claim ~~33~~ 1, wherein the first transistor which includes a dielectric layer of a first thickness and having a top layer which exhibits a high resistance to oxidation at high temperatures includes a top layer of silicon nitride (Si_3N_4) which comprises approximately a third of the first thickness of the dielectric layer.

~~40~~ 8. The structure of claim ~~33~~ 1, wherein the first transistor which includes a dielectric layer of a first thickness includes a dielectric layer having a thickness of less than 7 nanometers, wherein the dielectric layer has a bottom layer of silicon dioxide (SiO_2), and wherein the top layer is silicon nitride (Si_3N_4).

~~55~~ 9. (Amended) A logic device and a memory device structure on a single substrate, comprising:

a first transistor, wherein the first transistor includes:

a first dielectric layer of a first thickness less than 5 nanometers (nm);

a top layer which exhibits a high resistance to oxidation at high temperatures; and

a second transistor, wherein the second transistor includes a second dielectric layer of a second thickness different from the first thickness.

~~56~~ 10. The structure of claim ~~55~~ 9, wherein the first dielectric layer and the top layer together have a thickness of less than 7 nanometers (nm).

~~57~~ 11. The structure of claim ~~55~~ 9, wherein first dielectric layer of a first thickness includes silicon dioxide (SiO_2) and the top layer includes silicon nitride (Si_3N_4).

58. The structure of claim 55, wherein the second dielectric layer of a second thickness includes a dielectric layer formed entirely of silicon dioxide (SiO_2).

59. The structure of claim 55, wherein the second dielectric layer of a second thickness includes a dielectric layer having a thickness of less than 12 nanometers.

60. The structure of claim 55, wherein the top layer includes a top layer of silicon nitride (Si_3N_4) which comprises approximately a third of the first thickness of the first dielectric layer.

61. The structure of claim 55, wherein the top layer exhibits a high resistance to boron penetration at high temperatures.

62. (Amended) A logic device and a memory device structure on a single substrate, comprising:

a first transistor, wherein the first transistor includes:

a first dielectric layer of a first thickness less than 5 nanometers (nm);

a top layer which exhibits a high resistance to boron penetration at high temperatures; and

a second transistor, wherein the second transistor includes a second dielectric layer of a second thickness different from the first thickness.

63. The structure of claim 62, wherein the first dielectric layer and the top layer together have a thickness of less than 7 nanometers (nm).

64. The structure of claim 62, wherein first dielectric layer of a first thickness includes silicon dioxide (SiO_2) and the top layer includes silicon nitride (Si_3N_4).

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~~65~~. The structure of claim ~~62~~, wherein the second dielectric layer of a second thickness includes a dielectric layer formed entirely of silicon dioxide (SiO_2).

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~~66~~. The structure of claim ~~62~~, wherein the second dielectric layer of a second thickness includes a dielectric layer having a thickness of less than 12 nanometers.

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~~67~~. (Amended) A logic device and a memory device structure on a single substrate, comprising:

a first transistor, wherein the first transistor includes:

a first dielectric layer of a first thickness less than 5 nanometers (nm);

a silicon nitride (Si_3N_4) top layer which exhibits a high resistance to oxidation at high temperatures; and

a second transistor, wherein the second transistor includes a second dielectric layer of a second thickness different from the first thickness.

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~~68~~. The structure of claim ~~67~~, wherein the first dielectric layer and the top layer together have a thickness of less than 7 nanometers (nm).

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~~69~~. The structure of claim ~~67~~, wherein the second dielectric layer of a second thickness includes a dielectric layer formed entirely of silicon dioxide (SiO_2).

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~~70~~. The structure of claim ~~67~~, wherein the second dielectric layer of a second thickness includes a dielectric layer having a thickness of less than 12 nanometers.

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~~71~~. The structure of claim ~~67~~, wherein the silicon nitride (Si_3N_4) top layer includes a silicon nitride (Si_3N_4) top layer with a thickness of approximately a third of the first thickness of the first dielectric layer.

~~72~~ 26. The structure of claim ~~67~~ 21, wherein the top layer exhibits a high resistance to boron penetration at high temperatures.

~~73~~ 27. (Amended) A logic device and a memory device structure on a single substrate, comprising:

a first transistor, wherein the first transistor includes:

a first dielectric layer of a first thickness less than 5 nanometers (nm);

a top layer of approximately a third of the first thickness, which exhibits a high resistance oxidation at high temperatures; and

a second transistor, wherein the second transistor includes a second dielectric layer of a second thickness different from the first thickness.

~~74~~ 28. The structure of claim ~~73~~ 27, wherein the top layer exhibits a high resistance to boron penetration at high temperatures.

~~75~~ 29. The structure of claim ~~73~~ 27, wherein the first dielectric layer and the top layer together have a thickness of less than 7 nanometers (nm).

~~76~~ 30. The structure of claim ~~73~~ 27, wherein the second dielectric layer of a second thickness includes a dielectric layer formed entirely of silicon dioxide (SiO_2).

~~77~~ 31. The structure of claim ~~73~~ 27, wherein the second dielectric layer of a second thickness includes a dielectric layer having a thickness of less than 12 nanometers.

~~78~~ 32. (Amended) A logic device and a memory device structure on a single substrate, comprising:

a first transistor, wherein the first transistor includes:

a first dielectric layer of a first thickness less than 5 nanometers (nm);

a top layer which exhibits a high resistance to oxidation at high temperatures; and

a second transistor, wherein the second transistor includes a second dielectric layer of a second thickness different from the first thickness, wherein the second thickness is less than 12 nanometers (nm).

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~~79~~. The structure of claim ~~78~~, wherein the top layer exhibits a high resistance to boron penetration at high temperatures.

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~~80~~. The structure of claim ~~78~~, wherein the first dielectric layer and the top layer together have a thickness of less than 7 nanometers (nm).

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~~81~~. The structure of claim ~~78~~, wherein the second dielectric layer of a second thickness includes a dielectric layer formed entirely of silicon dioxide (SiO_2).

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~~82~~. (Amended) A logic device and a memory device structure on a single substrate, comprising:

a first transistor, wherein the first transistor includes:

a first dielectric layer of a first thickness less than 5 nanometers (nm);

a silicon nitride (Si_3N_4) top layer of approximately a third of the first thickness, which exhibits a high resistance to oxidation at high temperatures; and

a second transistor, wherein the second transistor includes a second dielectric layer of a second thickness different from the first thickness, wherein the second thickness is less than 12 nanometers (nm).

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~~83~~. The structure of claim ~~82~~, wherein the top layer exhibits a high resistance to boron penetration at high temperatures.

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~~84~~. The structure of claim ~~82~~, wherein the first dielectric layer and the top layer together have a thickness of less than 7 nanometers (nm).

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~~85~~. The structure of claim ~~82~~, wherein the second dielectric layer of a second thickness includes a dielectric layer formed entirely of silicon dioxide (SiO_2).

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~~86~~. (Amended) A logic device and a memory device structure on a single substrate formed by the method comprising:

forming a pair of transistor channel regions on the single substrate;

forming a pair of gate oxides to a first thickness on the pair of channel regions;

wherein forming the pair of gate oxides to a first thickness includes forming the pair of gate oxides to a thickness of less than 5 nanometers (nm) by krypton plasma generated atomic oxygen at approximately 400 degrees Celsius;

forming a thin dielectric layer on one of the pair of gate oxides, wherein the thin dielectric layer exhibits resistance to oxidation at high temperatures; and

forming the other of the pair of gate oxides to a second thickness different from the first thickness.